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M. Tech. Embedded Systems

End Semester Examination

Subject: Low Power VLSI Design

Sub Code: EES 509.1

Day and Date: Wednesday, 13/12/2017 **Total Marks:** 100

Time: 10:30 - 01:30

Instructions:

1. All questions are compulsory
2. Figures to the right indicate full marks.
3. Assume suitable data if necessary.

Q.1 Attempt any three of the following: **[3 x 6 = 18]**

a. Explain the need for low power VLSI chips CO1

b. Explain different source of power dissipation in digital Integrated Circuits CO1

c. What are the Emerging Low power approaches. Brief the basic principles of Low Power Design CO1

d. With respect to gate level logic simulation explain the following a) Capacitive Power dissipation b) Internal Switching Energy CO2

Q.2 Attempt any two of the following: **[2 x 8 = 16]**

a. Explain the Data Correlation Analysis in DSP Systems by taking dual bit type signal model. Take 'single-input single-output' example for characterization. CO2

b. With respect to Architecture-level Analysis explain a) Power Model Based on Activities b) Power model based on component operation CO2

c. Derive the expression for the minimum number of samples/simulations to be carried out for estimating the power in a digital circuit using Monte Carlo Simulation. CO2

Q.3 Attempt any two of the following: **[2 x 8 = 16]**

a. With reference to Gate reorganization explain the following

a) Local Restructuringb) Signal Gating CO3

b. With suitable example, explain a)State Machine Encoding b)Precomputation logic CO3

c. Explain Bus Invert Encoding with statistics. CO3

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Q.4 Attempt any three of the following: **[3 x 6 = 18]**

a. With a neat diagram explain 'Adaptive performance management by voltage control'. CO4

b. With a suitable example explain Adaptive Filtering. CO4

c. With a suitable example explain Loop Unrolling CO4

d. How parallel architecture can contribute for low power design? Explain with suitable statistics. CO4

Q.5 Attempt any two of the following: **[2 x 8 = 16]**

a. Explain Algorithmic level analysis and optimization for 'Vector Quantization' application CO5

b. Explain Architectural level analysis and optimization for 'FIR Filter' application CO5

c. With respect to Algorithmic level write short notes on

a) Power estimation b) Locality CO5

Q.6 Attempt any two of the following: **[2 x 8 = 16]**

a. Explain different types of software power estimation techniques CO6

b. With a suitable example explain how 'Algorithmic Transformations to match computational resources' helpful for power optimization. CO6

c. With a suitable example explain Graph-Partitioning method for memory bank assignment CO6

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